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METHOD OF INCREASING THE SAMPLING RATE OF THE PIC MICROCONTROLLERS ANALOG TO DIGITAL CONVERTER

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Abstract: *This paper presents a new method of increasing the speed of data acquisition for analog-digital converter of PIC microcontrollers. This method can be used to applications that do not work in real time. The paper describes the principle of the method, the design and the testing activities. Performances depend on the quality and the performances of the used components. The experiments show good results for control of variable reluctance stepper motors.*

Key words: *microcontroller, analog to digital conversion, conversion time, sampling rate, software.*

1. INTRODUCTION

Nowadays, the use of microcontrollers has spread widely on one hand due to the simplicity of their use, and on the other hand due to their increasing performances. The microcontrollers offer a wide range of peripherals included in their structure, thus making possible numerous command and control applications using a minimum of resources.

There are situations in which the acquiring of superior performances is required by the nature of the signals processed, or by the time restrictions [1 and 2].

The microcontroller systems or the programmable system-on-chip (PSoC) structures used nowadays in the embedded systems are fitted with analog-digital converters with successive approximation or with delta modulation, which are included in the chip. The acquisition speed of these converters depends on the maximum CPU clock frequency. Modern external analogue converters are required in order to achieve analogue to digital conversions at speeds that are higher than the maximum speed.

This paper presents a cheaper solution for increasing the acquisition speed over the maximum limit using the existing digital analogue converter. The proposed method allows digital to analog acquisition over the maximum limit by acquiring the higher-speed analog signal with an external circuit and converting the signal acquired with the existing low speed ADC.

The main disadvantage of this method is the fact that the sampling is not done continually, and thus results cannot be obtained in real time. The sampling is done by acquiring a number of high-speed samples, and by storing the voltages of the samples in capacitors, and then by converting the voltages of the storing capacitors with the help of the A/D converter included in the microcontroller at its maximum speed. This method allows the acquiring of the signals with superior sampling rates as opposed to the one offered by the A/D converter included in the microcontroller.

Moreover, the principle of this method states that the microcontroller has to achieve through the program certain improvements on the converted signals, so that they are precise.

2. DETAILING OF THE CURRENT SITUATION AND THE IMPROVEMENTS PROPOSED

The middle class PIC microchip microcontrollers are equipped with an analog digital converter that can acquire analog signals with a 10 bits resolution. According to the manufacturer's specifications [3] the following equation gives the duration of a sampling:

$$t_{AD} = t_{acq} + t_{conv}\,. \tag{1}$$

where: t_{AD} is A/D sample time, t_{acq} is acquisition time and t_{conv} is A/D conversion time.

For the analog-digital converter with which the middle class PIC Microchip controllers (PICmicro Mid-Range MCU Family) are equipped, the acquisition time, marked from now on T_{acq}, is given by the equation 2:

$$t_{acq} = t_{amp} + t_{C} + t_{coff}\,. \tag{2}$$

where: t_{amp} is amplifier setting time, t_C is holding capacitor-charging time and t_{coff} is temperature coefficient. The equation 2 shows a minimal acquisition time of 19.72 μs at a maximum terminating resistance of 10 kΩ. If the load resistance is 50 Ω (the minimum value), then the acquisition time of a sampling decreases at 10.61 μs [3].

In [3], in order to compute the conversion time (A/D Conversion Time), the starting point is the conversion time marked as T_{AD}. For a correct conversion, the minimum value of 1.6 μs for T_{AD} must be applied. In addition, in [3] it is shown that the conversion of 10 bits requires an acquisition time of $11.5T_{AD}$. An additional delaying time of $2T_{AD}$ is added to this value before the beginning of a new acquisition.

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This way, using the minimum values and equation (1), the following result is obtained: A/D Sample Time = 10.61 μs + 13.5 * 1.6 μs = 32.21 μs which corresponds with a sampling frequency of 3.10 ksps (kilo samples per second). If, for example, we want to sample a signal with 32 samples per period, then the maximum frequency of the input signal will be approximately 97 Hz.

This article frames a method intended to acquire frequency signals superior to this frequency, but not in real time, which can be inconvenient in some cases. The method can be useful though, in the recording of the rapid phenomena by "photographing" and labeling them for further study. Sampling frequencies superior with a few magnitudes to the ones obtained through the direct use of the A/D incorporated converter can be obtained through the use of the middle class PIC microcontroller and of the appropriate components with a high switching speed.

3. THE DESCRIPTION OF THE CIRCUIT FOR THE SIGNAL ACQUISITION

The principle block diagram of the circuit for the acquisition of the rapid variation signal in time is shown in Fig. 1.

The acquisition of the signal is performed in two stages. In the first stage the swa1 switch is in "acquisition" position and the input signal "signal IN" is stored in C capacitors. The input signal is sampled by the swa2 switch which is controlled by the appropriate frequency rate of the input signal.

In the second stage, the signal stored in the C capacitors is converted by the internal ADC (analog to digital converter) of the microcontrollers into numeric values. This time the swa1 switch is on "conversion" position and the swa2 switch is set at maximum frequency of the microcontroller's internal ADC. The principle of operation is based on the separate sampling of the signal at a high frequency and its conversion at the maximum attainable frequency by the A/D converter of the microcontroller [4–7]. The diagram of the principle for the acquisition system is presented in Fig. 2.

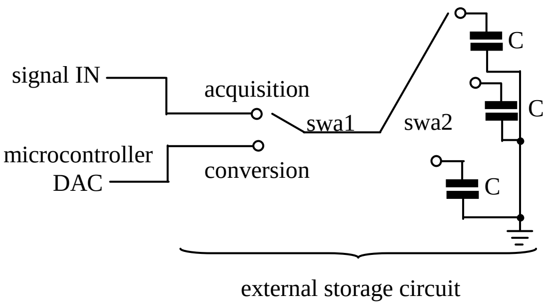

Fig. 1. The principle block diagram.

The acquisition of the signal is done in two stages. The first one is the "photographing" of the signals, which is then recorded in the C1-C8 capacitors. For this, the microcontroller switches the SWA1 analog switch on "1", so that the analog signal which has to be recorded in the C1–C7 capacitors is applied at the access point of the analog demultiplexer.

The control of the SWA1 switch is done through the signal of the CMD1, which is supplied by the digital PORTB exit of the microcontroller. The sampling frequency of the signal at the entry point, marked in Fig. 2 as "Signal IN" is established with the help of the 5 bits CMD2 signal, constituted from the digital PORTB.2-PORTB.6 exits of the U1 microcontroller. This way, the selection of 32 different frequencies is possible. Figure 2 presents the f1–f5 sampling frequencies and the f_{ach} for the acquisition of the sampled voltages supplied by the U4 circuit. The U4 circuit is obtained from a quartz crystal oscillator and a numeric frequency divider represented by a binary numerator. The *f1* frequency is the highest and the f_{ach} is the lowest.

The f_{ach} frequency corresponds to the maximum acquisition speed of the analog-digital converter of the U1 microcontroller. The other frequencies, which are superior to the f_{ach} frequency, are used for the acquisition ("photographing") of the "Signal IN" signal at the entry point. From these frequencies, only one is selected through the SWD1 circuit controlled by the CMD2 signal. After this selection, the supplying of the signal at the exits of the U4 circuit is validated through the deactivation of the reset RST signal sent from the digital entry PORTB.7 of the U1 microcontroller. The exit signal of the SWD1 circuit, which is one of the selected frequencies, forms the command signal CMD3 for the SWA2

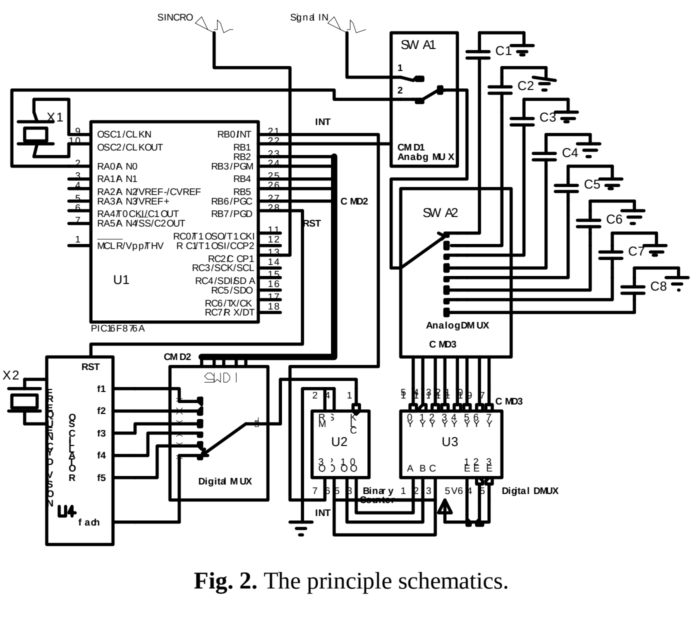

Fig. 2. The principle schematics.

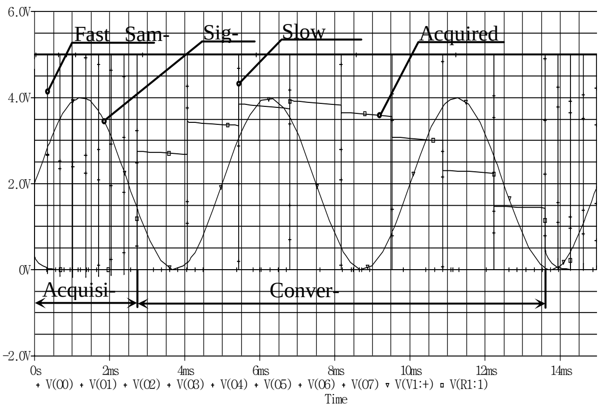

Fig. 3. The obtained wave forms.

circuit through the U2 binary numerator and the U3 digital demultiplexer.

Because the SWA2 circuit is a digital demultiplexer, the result is that the frequency selected represents in fact the sampling frequency of the entry signal Signal IN. The values of the entry signal are recorded in the C1–C8 capacitors, and at the end of the caption cycle, the U2 circuit generates an interrupt signal on the INT(PORTB.0) entry of the microcontroller, to flag this event. At the appearance of the interrupt, the second conversion phase of the acquired signal (stored in the C1-C8 capacitors) begins.

In this phase, the microcontroller activates the RST signal in order to stop the U4 circuit from supplying oscillations, and switches SWA1 on position 2, selecting the f_{ach} frequency with the help of SWD1, which coincides with the maximum conversion speed of the inner analog-digital converter and deactivates the RST signal in order to permit the supply of the f_{ach} signal by the U4 circuit and the beginning of the conversion of the stored voltages from the C1–C8 capacitors. At the end of this phase, the acquired signal is converted and stored in the RAM memory of the microcontroller and a new interrupt, which prepares the recommencing of the cycle, is generated. The main forms of waves for this circuit are shown in Fig. 3.

The sequence described above can be automatically repeated, a chain of acquired signals being thus obtained. These signals can be stored in a serial memory attached to the microcontroller (for example a MMC or SD memory) or they can be sent through the serial port or USB to a computer.

Moreover, the circuit has the possibility of synchronization of the acquisition signal “Signal IN” through the internal comparator module with which the microcontroller is equipped. The entry signal in the comparator module is the “SINCRO” signal. The moment, in which the “SINCRO” signal surpasses the internal reference installed by the program, an interrupt that triggers the acquisition process of the signal is generated.

4. A FEW REMARKS ON THE ENGINEERING OF THE CIRCUIT

The making of the acquisition circuit, which constitutes of an analog switch and a storing capacitor of the acquired sampling, entails some engineering restrictions, which will be presented below (Fig. 4).

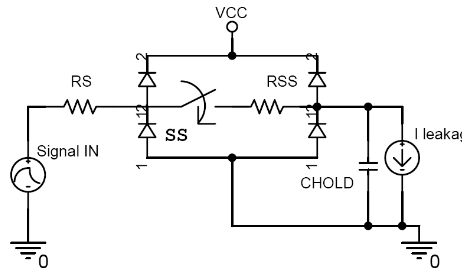

Fig. 4. The equivalent diagram of the analog switch.

The maximum acquisition time of a signal sampling is given by a relation similar to relation (1). For example, if we take an equivalent diagram for the analog switch as the one in Fig. 4, and in the situation in which we consider that the maximum error permitted is ½ LSb (for 1024 steps of the A/D converter), we have the following equation:

$$U_{C_{HOLD}} = \left(V_{CC} - \frac{V_{CC}}{2048}\right)\left(1 - e^{\frac{-t}{(R_S + R_{SS})C_{HOLD}}}\right),$$

$$t_{acq} = -C_{HOLD}\left(R_S + R_{SS}\right)\ln\left(\frac{1}{2047}\right). \tag{3}$$

The selection of the C_{HOLD} capacitor is done by taking into consideration the following requisites: on one hand, C_{HOLD} has to have the smallest value possible in order to ensure the lowest acquisition time, and on the other hand, C_{HOLD} has to have a high enough value to maintain the voltage value at its terminals until its conversion by the A/D converter of the microcontroller is done.

After the analog converter opens, the discharge of the C_{HOLD} capacitor is basically done due to the Maximum Switch OFF Leakage Current (Fig. 4), current which, if we consider constant, will produce a variation of the voltage at the terminals of the capacitor, variation given by Eq. (4).

$$\Delta U_{C_{HOLD}}(t) = \frac{I_{leakage}}{C_{HOLD}}\, t\,. \tag{4}$$

According to Fig. 3, the time elapsed from the moment when the C_{HOLD} capacitor is loaded with the value of the voltage at the entry (Signal IN) until this voltage is converted by the A/D converter of the microcontroller, is given by Eq. (5).

$$t_i = (n - i - 1)t_a + it_c\,, \tag{5}$$

where: t_i is the time for the capacitor value maintaining, n is the number of sampling gathered in a session (in Fig. 2, n = 8), i is the number of sampling (i = 0, 1, 2...n-1), t_a is the acquisition time, t_c is the conversion time. These durations are different for every sampling and the maximum duration is obtained for i = n when t_n = (n-1) tc.

The duration of a complete acquisition and conversion cycle of n samplings will be given by the Eq. (6):

$$T_{shot} = n\,t_a + n\,t_c\,, \tag{6}$$

or, we can acquire a chain of n samplings at intervals equal to T_{shot}.

The discharge of the capacitor in the time span between the acquisition moment and the conversion moment introduces an error that depends both on the characteristics of the analog switch and on the chosen sampling frequency.

In order to eliminate these errors, the entry signal is adapted through the adding of a sequential component which has the maximum value of the voltage variation on the C_{HOLD} capacitor in the worst case scenario (the lowest sampling frequency) and is enclosed in the 0–5 V domain sustained by the A/D incorporated converter of the microcontroller.

Before the start of the acquisition proper of the entry signal, for every rated sampling sequence, an auto calibration through a program of the acquisition circuit is done (the auto calibration circuit was not depicted in Fig. 2).

For this to be done, the maximum acquisition voltage (V_{CC}) is applied at the entry point of the circuit, thus a complete cycle of acquisition and conversion is completed.

The converted values, read in the RAM memory, differ from the real ones because of the differences between the electronic switches that form the acquisition circuit and because of the discharge of the C_{HOLD} capacitor while it waits for the conversion to start.

The difference between the real value and the one measured during the calibration is stored in the EPROM memory of the microcontroller (the number of the values obtained is equal to the number of samplings gathered during a cycle) and it is kept during the whole period in which acquisitions with that particular sampling frequency are done. During the acquisition of the real signal (Signal IN), each acquired sampling from a cycle of n samplings is being redressed according to the value stored in the EPROM memory before being stored in the RAM memory or before being sent further along.

5. THE ACQUISITION SOFTWARE

The software for the central unit of the system controls the three phases of acquisition: the activation, the acquisition phase and the final stage.

In the activation phase, the way in which the acquisition is made (synchronous or asynchronous), the number of samplings of a cycle, the number of cycles, the sampling frequency and the storing method of the result is chosen and the auto calibration is achieved.

In the acquisition phase, the storing process of the samplings in the capacitors is triggered, the process being either synchronous or asynchronous depending on the option made in the activation phase, after which the conversion process starts. As the conversion takes place, each sampling is redressed with the data from the EPROM memory and it is recorded or transmitted through the serial interface or the USB port.

In the final stage, the cycle is recommenced in the case that in the activation phase, the acquisition of several cycles of samplings was specified, or in the case that the process stops and the saving of the data is finalized (the folders are closed, the ending signal is sent, etc.).

6. CONCLUSIONS

Advantages of the presented method consist in the expanding of the analog to digital acquisition performance of the simple digital systems. The method can be extended to performance systems for further increase their performance.

The solution presented above for the increase of the sampling speed of the A/D incorporated converter of the PIC microcontrollers can be useful where the monitoring of the signal can be made at certain periods of time. Although the signal conversion is not done in real time, the moment in which the result is obtained is relatively close to the moment of the signal acquisition.

For example, through the use of the MM54HC4016 analog switches, a maximum sampling frequency of 21 ksps was obtained. At this frequency, the maximum time period elapsed from the moment of the sampling acquisition to the moment of its conversion is 255 μs, when 8 samplings per cycle are acquired.

This circuit was used with great results for the stepper motors with variable reluctance, through the computing of the charge at the shaft from the speed of the inductivity of the motor phase [8 and 9].

Circuits with superior performances can be used with great results at the recording of the transient phenomena that appear at the electric power switches in order to improve their reliability.

REFERENCES

[1] C.D. Cîrstea, S.I. Buda, F. Constantin, *Data acquisition system*, Romanian Reports in Physics, Vol. 57, No. 3, 2005, pp. 376–381.

[2] P. Asimakopoulos, G. Kaltsas, and A.G. Nassiopoulou, *A microcontroller-based interface circuit for data acquisition and control of a micromechanical thermal flow sensor*, Journal of Physics: Conference Series 10, 2005, pp. 301–304.

[3] Microchip Technology Inc., *PICmicro Mid-Range MCU Family Reference Manual*, Microchip, Corporate Headquarters Microchip Technology Inc., Arizona, USA, 2002.

[4] P. Quinn, M. Pribytko, *Capacitor matching insensitive algorithmic ADC requiring no calibrations*, Integration, the VLSI Journal, Vol. 36, Iss. 4, November 2003, pp. 211–228.

[5] P. Carbone, D. Petri, *Design of ADC sinewave histogram test*, Computer Standards & Interfaces, Vol. 22, Iss. 4, 2000, pp. 239–244.

[6] L. Michaeli, P. Michalko, J. Saliga, *A new ADC fast testing method based on the unified error model*, *Measurement*, Advances in Measurements of Electrical Quantities, Vol. 41, Iss. 2, February 2008, pp. 192–197.

[7] P. Arpaia, P. Daponte, S. Rapuano, *A state of the art on ADC modelling*, Computer Standards & Interfaces, Vol. 26, Iss. 1, 2004, pp. 31–42.

[8] D. Rotar, *Inductive position Sensor for Switched Reluctance Motor*, International Conference on Communications, Signals and Systems, AMSE, pp. 343–346, Brno, Czech Republic, September 1996, Faculty of Electrical Engineering and Computer Science, Brno.

[9] D. Rotar, Ş. Ababei, *Advanced flexible virtual instrument with PIC microcontroller*, CNEI 2009, Proceedings of the 7th national conference on industrial energetics with international participation, pp. 467–472, November 2009, Universitatea din Bacău, Bacău, Romania.