Proceedings in MANUFACTURING SYSTEMS

Proceedings in Manufacturing Systems, Volume 7, Issue 2, 2012 ISSN 2067-9238

MEMS MANUFACTURING AND RELIABILITY

Titu-Marius BĂJENESCU[1,*], Marius BÂZU[2]

[1)] Prof., Reliability Consultant, C. F. C., La Conversion, Switzerland
[2)] PhD, Head of Reliability Laboratory, IMT-Bucharest, Romania

Abstract: *The Micro Electro Mechanical Systems (MEMS) are among the most promising areas in future computer and machinery, the next logical step in the silicon revolution. But the MEMS industry is currently at a much more vulnerable position than it appears, regardless of how wonderful its future may looks like. A full understanding of the physics and statistics of the defect generation is required to investigate the ultimate reliability limitations for MEMS. Biggest challenge: cost effective, high volume production. Within MEMS technological expansion, device manufacturing costs, failure and long-term performance reliability are critical issues that have to be resolved using basic probabilistic design methodologies which are largely unexploited by industrial companies at the mature innovation level. There are a number of factors that contribute to the reliability of MEMS: packaging (in particular, in bonding and sealing), material characterization relating to operating and environmental conditions, credible design considerations, the techniques for mitigating intrinsic stresses/strains induced by fabrications and testing for reliability are a few of these factors. The reliability aspect includes both the electronic and the mechanical parts, complicated by the interactions. Reliability is a critical issue in any industrial and consumer product development. MEMS devices are becoming essential components of modern engineering systems and their reliability is of particular importance in applications where their failure can be catastrophic and devastating.*

Key words: *fabrication, failure mechanisms, failure analysis, MEMS, packaging, reliability.*

1. INTRODUCTION

Microsystems are miniaturized devices which perform non-electronic functions, such as sensing and actuation, fabricated by IC compatible (CMOS) batch-processing techniques [1]. They are integrating electrical components (e.g. capacitors, piezoresistors), mechanical components (e.g. cantilevers, micro switches), optical components (e.g. micro mirrors) or fluidic components (e g. flow sensors). Initially, synonyms for microsystems were micro electro mechanical systems (MEMS), used mainly in the United States and Europe, or micro machines (in Japan).

Cost effective packaging and reliability are two critical factors for successful commercialization of microsystems. While packaging contributes to the effective production cost of MEMS devices, reliability addresses consumer's confidence in and expectation on sustainable performance of the products [2]. MEMS[1] products are designed to perform a variety of functions of electromechanical, chemical, optical, biological and thermo-hydraulic natures. Mechanisms that cause failure of MEMS devices thus vary significantly from one type to another. Design for reliability of these devices is also significantly different from most other engineering systems.

Integration of process engineering, design, yield engineering, reliability, characterization and test from the early development phases through to product release and into manufacturing is an effective model for success in the MEMS industry.

2. EVALUATING THE RELIABILITY

Two procedures were proposed for evaluating MEMS reliability [3]:

- To evaluate the reliability of a Virtual Prototype, i.e. simulating the dependence of the reliability level on device structure and process parameters;
- To shorten the test time by using accelerated testing, this means to test the components at higher values of stress as those encountered in normal functioning, in the aim to shorten the time period necessary to obtain significant results. These two solutions are complementary, because the estimations made on a Virtual Prototype has to be verified by the accelerated testing.

The combination of electrical and non-electrical properties in these systems presents a challenge to test and characterization. Alongside traditional electrical test procedures, non-electrical tests, optical measurement and stimulation processes in particular are also utilized. The integration of special instruments, such as laser vibrometers, spectrometers, interferometers or spectrophotometers, makes possible a combined electrical and mechanical/optical characterization of the microsystems. The electrical control is carried out with mixed-signal test systems, which in turn offer convenient program creation, a large degree of flexibility and high test coverage.

[*] Corresponding author: C. F. C., La Conversion, Switzerland
E-mail address: *tmbajenesco@bluewin.ch*

1 Examples of MEMS device applications include inkjet-printer cartridges, accelerometers, miniature robots, micro-engines, locks, inertial sensors, micro-transmissions, micromirrors, micro actuators, optical scanners, fluid pumps, transducers, and chemical, pressure and flow sensors. New applications are emerging as the existing technology is applied to the miniaturization and integration of conventional devices.

3. FAILURE MECHANISMS

In Tables 1 and 2, the most important failure mechanisms (FMs) of MEMS are synthesized, grouped according the source of failure risks: the material and the design and fabrication, respectively.

In each case, the possible corrective actions are mentioned, because the final goal of any reliability study is

Table 1

Failure mechanisms depending on material quality [3].

Failure mechanisms	Recommended corrective actions
Silicon crystal irregularities could initiate, after etching (DRIE), protuberances that may obstruct the movement of the moving elements of the microsystem, leading to failure. High-resolution x-ray diffraction methods such as the rocking curve method and reciprocal space mapping can monitor crystalline imperfection in single crystal silicon devices.	Thermal annealing improves the crystal quality, removing some crystal irregularities.
Surface roughness coupled with the limiting capacity of some micro fabrication process such as DRIE for deep trench etching in silicon substrates can introduce significant fitting problems during assembly.	Optimization of DRIE may diminish the failure risks.
The *mismatched CTE* between layers of thin films of dissimilar materials may induce significant failure risks, especially after long- term thermal cycling.	The materials in contact must be carefully chosen.
The *variations* in material parameters (e.g., resistivity change in materials due to thermally induced resistance during operation) may lead to failure.	An adequate choice of the used material may avoid this FM.
The *internal stresses* in materials induce significant failure risks. This is a temperature- dependent process.	Temperature changes must be minimized by adequate process design.
Polymers and plastics are associated with a major reliability problem: degradation by *aging with time* : they harden with time, resulting in continuous change of material characteristics, leading to malfunction of the devices (e.g. malfunction of pressure microsensors using polymer protection coatings to silicon die).	Carefully chose the material for a given application.
Polymers and plastics continue to release gases after being sealed in packages. Outgassing of materials and device operation itself may lead to *clogging* or build-up of material in strategic active regions. This is detrimental in microfluidics, making the device inoperable by obstructing or restricting the fluid flow.	Carefully chose the material for a given application.

Table 2

Failure mechanisms depending on design and fabrication processes [3]

Failure mechanisms	Recommended corrective actions
FMs specific to the operation of *releasing the suspended parts* of the microsystem (membranes, beams, etc.): *(i)* A *partial release* (meaning the suspended part was not totally released from the surrounding material) could be initiated by insufficient etching, oxide residuals that prevent adequate etching, slow etching rate because of an inadequate solution or by redepositions of etched materials; *(ii)* The *break of the part* due to mechanical rupture.	Using control and monitoring points on the manufacturing flow.
Some FMs are induced by *etching operation*: *(i)* Buckling is due to residual stresses and is observed in MEMS during etching of the underlying sacrificial layer. Buckling is the deformation induced by thermal strain; *(ii)* Residual stresses induce plastic deformation/displacement by relaxation.	Using control and monitoring points on the manufacturing flow.
TDDB, explained by a percolation model. An electric field applied to an oxide film causes the injection of holes into the oxide film to occur on the anode side, and it consequently causes traps to be made in the oxide film. As the number of traps increases, an electric current via the traps is observed as an stress induced leakage current (SILC) due to hopping or tunneling. It has been reported that if the number of traps continues to increase and the traps connect between the gate electrode and the Si substrate, the connection carries a high current that causes the gate oxide film to break down.	The level of the traps in an oxide film strongly influences TDDB, and it is necessary to characterize the oxide film quality with accelerated tests and feed the results into design rules. Also, it is important to use SiO_2 film, which does not easily produce defects, and to develop a method of forming an oxide film thereby.
Particle contamination (produced by environment pollution and alteration) may mechanically obstruct the device motion, resulting in electrically short-out device. The contamination could happen in packaging and during storage, for example, a particulate dust that lands of one of the electrodes of a comb drive can cause catastrophic failure.	Sources of particle contamination, such as residues left after fabrication and wear-induced debris or environmental contaminations, must be eliminated.
Electromigration, which is specific for IC technology, may also arise for microsystems. It is caused at high-current densities, by the gradual displacement of metals atoms, causing a change of conductor dimensions, and, eventually, high resistive spots and failure due to destruction of the conductor at these spots.	Appropriate design rules may diminish or eliminate such failure risks.
Stiction is typical for solid objects that are in contact during operation.	Stiction is detailed below.
FMs related to the presence of *mechanical movement*, which introduces new classes of reliability issues that are not found in traditional devices; e.g. are cycled mechanical deformations and steady-state vibrations, which introduce new stress mechanisms on the structural parts of these devices.	Mechanical relaxation of residual material stress, plastic deformations under large signal regime, creep formations and fatigue can all cause device mechanical failure.

not only to evaluate, but also to improve the reliability level of the product. As indicated in Table 2, some details about stiction are following.

Stiction is an informal expression for 'static friction', describing the phenomenon that makes two parallel plates pressing against each other to stick together. Some threshold of force is needed in order to overcome this static cohesion. The Van der Waals forces are a possible cause of stiction. These are attractive or repulsive forces between molecules (other than covalent bonds or electrostatic interactions of ions with one another or with neutral molecules) and include: *(i)* Forces between permanent dipoles, *(ii)* Forces between permanent dipole and induced dipole, and *(iii)* Forces between instantaneous induced dipole and induced dipole. The hydrogen bond could also be responsible for stiction: this is the attractive force between the hydrogen attached to an electronegative atom of one molecule and an electronegative atom of a different molecule. Other possible causes of stiction are the electrostatic forces or solid bridging. If arising during operation, the stiction may lead to electrostatic discharge that causes arcing between electrode surfaces and, eventually, micro-welding. Humidity is a detrimental factor, by changing surface properties, and favoring stiction between the surfaces. It is possible to avoid stiction by using surface assembly monolayers or by designing low-energy surfaces [5].

4. CRITICAL DIMENSIONS

The scanning electron microscope (SEM) as applied to critical dimensions (CD) metrology and associated characterization modes such as electron beam-induced current and cathodo-luminescence (CL) has proved to be a workhorse for the semiconductor industry during the microelectronics era. In [5], some of the challenges facing these techniques in light of the silicon nanotechnology road map are reviewed and new results using voltage contrast imaging and CL spectroscopy of top-down fabricated silicon nanopillar / nanowires (<100 nm diameter) are presented, which highlight the visualization challenge. However, both techniques offer the promise of providing process characterization on the 10-20 nm scale with existing technology. Visualization at the 1 nm scale with these techniques may have to wait for aberration-corrected SEM to become more widely available. Basic secondary electron imaging and CD applications may be separately addressed by the He-ion microscope.

MEMS are manufactured by microtechnologies. But when speaking about MEMS, the term "nanotechnology" has to be mentioned too, because of the current direction in microtechnology researches, going towards smaller and smaller dimensions.

Nanotechnology is predicted to create the sixth Kondratieff period following the "Age of Information". It represents a new revolutionary approach in fundamental research moving from a macrocentric to nanocentric system. Nanotechnology is expected to stimulate 1 trillion dollars of production involving about 2 million workers in the next 10 to 15 years. Today, more than 40 countries have specific nanotechnology research funding programs with the common goal of finding greater uses for the emerging technologies and enacting measures to encourage commercialization [6].

5. FAILURE ANALYSIS

The behavior of micro and nanoscaled products is extremely sensitive to changes in material compositions, manufacturing controllable variables, and noise parameters. The ultimate goal of manufacturing is to produce functional chips at continually higher volume and lower cost. Improvements in functional volume can be achieved by increasing wafer size, by decreasing die size through decreased critical dimensions, or by designing ICs for manufacturability with an eye toward a reduction in critical area. However, the most productive method is by improving the total die yield[2]. There are only four basic operations required to produce an IC: layering, patterning, doping, and heat treatment. In modern IC processing these four steps are repeated in over two hundred discrete processing steps in an infinite number of combinations, and each one of these steps are potential defect contributors that can reduce the total yield. One estimate suggested that particles are responsible for 75% of total yield loss in volume IC manufacturing [7]. Defect studying (i.e. defect inspection, defect classification, and defect source identification) is a crucial part of every modern IC fabrication. By necessity, advances in particle detection technology have kept pace with overall technology development.

Failure Analysis (FA) plays a very important role in the semiconductor industry in enabling timely product time-to-market and world-class manufacturing standards. Today ICs contain transistors having minimum geometries of 90 nm, but the industry is now rapidly moving into the 65 nm technology node. The actually chips contain hundreds of millions of transistors and operate at frequencies greater than 5 GHz. In general, the investigation of failures is a vital, but complex task.

From a technical perspective, failure can be defined as the cessation of function or usefulness. It follows that FA is the process of investigating such a failure. FA is an investigation of failure modes and mechanisms using optical, electrical, physical, and chemical analysis techniques. A number of tools and techniques enable analysis of circuits where, for example, additional interconnection levels, power distribution planes, or flip chip packaging completely eliminate the possibility of employing standard optical or voltage contrast FA techniques without destructive deprocessing [4]. The defect localization utilizes techniques based on advanced imaging, and on the interaction of various probes with the electrical behavior of devices and defects. In the recent years, various contributions to the reliability of nanodevices have been reported [8] provided basic physical modeling for MOSFET devices based on the nanolevel degradation that takes place at defect sites in the MOSFET gate oxide. The authors investigated the distribution of hot-electron activation energies, and derived a logistic mix-

[2] Die yield is the percentage of total die successfully manufactured, from silicon processing all the way through packaging and testing. Die yield is a function of manufacturing yield, test yield, package yield, and occasionally burn in yield. Since test, package, and burn in yield are typically close to unity, the die yield effectively becomes the manufacturing yield. For a given technology, reductions in defect density improve manufacturing yield. As technologies shrink, feature sizes decrease, and as feature sizes decrease, the size of a defect that can cause a functional failure decreases as well.

ture distribution using physical principles on the nanoscale.

The reliability of MEMS can be extremely sensitive to the environmental conditions, which translates in very stringent demands for the design, the materials used, and the package. Reliability must be built into the device at the design and manufacturing process stages. In most practical cases, the final damage quite rarely reveals a direct physical failure mechanism; often the original cause (or complete scenario of failure) is hidden by secondary post damage processes. On the other side, it is impossible to eradicate failures during the manufacturing process and at field use. Therefore, FA must be performed to provide timely information to prevent the recurrence of similar failures. Or, wafer fabrication and assembly process involves numerous steps using various types of materials. This, combined with the fact that devices are used in a variety of environments, requires a wide range of knowledge about the design and manufacturing processes. This explains while FA of semiconductor device is becoming increasingly difficult as VLSI technology evolves toward smaller features and semiconductor device structures become more complex. Since it is usually not possible to repair faulty component devices in a VLSI, each device in a chip can become a single point of failure unless some redundancy is introduced. Therefore, VLSIs have to be designed based on the characteristics of worst devices rather than those of average devices. Even if a chip is equipped with some redundant devices, today's scale of integration is becoming so high, that the yield requirement is still very severe. The final chip yield is governed by the device yield. A recent paper [9] demonstrates that once the major cause of failure is somehow identified or assumed, one could use a Monte Carlo method to study yield problems, even when the probabilities of interest differ from one another by many orders of magnitude. The method proposed in [9] was applied to the analysis of the leakage current distribution of double-gate MOSFETs; the microscopic FM that limits the final yield was identified. It explains experimental data very well. The insight into the FM gives clear guidelines for yield enhancement and facilitates device design together with the quantitative yield prediction. It is useful for yield prediction and device design. Transistors should be designed such that I_t (the maximum current generated by a single trap) is very much lower than the tolerable leakage current at the specified cumulative probability. The method does not have any convergence problems, as in the conventional Monte Carlo approach.

As long as aggressive designs are produced on cutting edge new manufacturing processes, there will be designs that don't work perfectly the first time on silicon or have low yields. Diagnosis and fail mode analysis by themselves can not complete the root cause process. Even if designs worked first time on silicon with reasonable yields, economic consideration of higher profitability, time-to-market and larger market share will drive continuous improvement of product performance, faster manufacturing ramps and higher yields. The question is: how to make the whole process of root-causing failures better, faster and cheaper? FA has implications on investment, required skills of the analyst, lab organization and time to result; the resulting cost explosion in FA cannot be compensated by any conceivable measures to enhance FA productivity, but this suppose that a rising number of today's FA problems will be solved by modern testing techniques. FA becomes such a substantial cost factor in yield learning, that testing must be empowered to do the FA job as well. It is important to integrate FA in semiconductor product and technology development and to introduce it as part of all new projects. This explains while, in the future, analysis productivity will be a key issue for product cost reduction [10]. More reliable electronic systems with high integrated functionality within a shorter period of development time, new methods/models for reliability of components and materials, and lifetime prediction are necessary. Reliability assurance has to be continued during the production phase, coordinated with other quality assurance activities. In particular: for monitoring and controlling production processes, item configuration, in process and final tests, screening procedures, and collection, analysis and correction of defects and failures. The last measure yields to a learning process whose purpose is to optimize the quality of manufacture, taking into account cost and time schedule limitations.

Today, FA is the key method in reliability analysis. It is impossible to conceive a serious investigation about the reliability of a product or process without reliability analysis. The idea that the failure acceleration by various stress factors (which is the clue of the accelerated testing) could be modeled only for the population affected by a single failure mechanisms greatly promoted FA as the only way to separate these population damaged by specific failure mechanisms.

A large range of methods are now used, starting from the (classical) visual inspection and going to such expensive and sophisticated methods as Transmission Electron Microscopy or Secondary Ion Mass Spectroscopy, etc.

A prognostic about the evolution of FA in the next five years is both easy and difficult to be made. Easy: because everyone working in this domain can see the current trend. Now the FA is still in a "romantic" period, with fabulous pictures or smart figures smashing the customers, convinced by such a "scientific" approach. Seldom, these users of electronic components do understand the essence of the FA procedure, because the logic is frequently missing.

But this situation is only a temporary one. Very soon, the procedures for executing FA will be stabilized and standardized, allowing to any user of an electronic component to verify the reliability of the purchased product.

It is also difficult to predict the evolution of FA [11], because the continuous progress in microelectronics and microtechnologies makes almost impossible to foresee with maximum accuracy the types of electronic components that will be most successful on the market. And the FA must serve this development, being one step ahead and furnishing to the manufacturers the necessary tools for their researches.

However, with sufficiently high probability one may say that the nanodevices (or even nanosystems) will become a reality in the next 5 years, so we have to be prepared to go deeper inside the matter, with more and more expensive investigation tools.

Recent advances in the design of MEMS have increased the demand for more reliable microscale structures. Although silicon is an effective and widely used structural material at the microscale, it is very brittle. Consequently, reliability is a limiting factor for commercial and defense applications. Since the surface to volume ratio of these structural films is very large, classical models for failure modes in bulk materials cannot always be applied[3].

The reliability of MEMS is directly related to the occurrence and severity of failures occurring at the manufacturing, operation of the device. It is surprising that little has been done to fully classify these failures. A methodology is also proposed in [12] to assess their severity and high level design of failures is implemented in the case of a thermal actuator.

As the design of MEMS devices matures and their application extends to critical areas, the issues of reliability and long-term survivability become increasingly important. Packaging of MEMS is an art rather than a science; the diversity of MEMS applications places a significant burden on packaging [13] (standards do not exist in MEMS packaging).

6. PACKAGING

Packaging has often been referred as the "Achilles heel of MEMS manufacturing" and a key bottleneck in the process of MEMS commercialization. At present, packaging is one of the major technical barriers that has caused long development times and high-costs of MEMS products. Other than the few fully commercialized products (i.e. air bag triggers, ink-jet print-heads, pressure sensors and a few medical devices), packaging constitutes the single largest element of cost and a major limitation to the miniaturization potential [13]. No MEMS product is complete unless it is fully packaged. At present, packaging is one of the major technical barriers that has caused long development times and high-costs of MEMS products. Heat-transfer analysis and thermal management become more complex by packing different functional components into a tight space. The miniaturization also raises issues such as coupling between system configurations and the overall heat dissipation to environment. Packaging involves bringing together

- Multitude of design geometries of the various constituent parts;
- Interfacing diverse materials;
- Providing required input/output connections, and
- Optimization of all of these for performance, cost and reliability.

On the other hand, reliability depends on:

(1) mutual compatibility of the various parts with respect to the desired functionality, and

(2) design and materials from the standpoint of long-term repeatability and performance accuracy.

[3] For example, whereas bulk silicon is immune to cyclic fatigue failure, thin micron-scale structural films of silicon appear to be highly susceptible. It is clear that at these size scales, surface effects may become dominant in controlling mechanical properties.

Reliability testing provides techniques for compensation, and an understanding of the catastrophic failure mechanisms in microsystems [14,15]. Engineers cannot design reliable MEMS without first to understand the many possible mechanisms that can cause the failure of the structure and performance of these devices and systems. And design alone cannot ensure the reliability of the product. It is imperative that the successful design and realization of microsystems or MEMS products must include all levels of packaging and reliability issues from the onset of the project. Besides fabrication related issues, packaging encompasses several other aspects that have also affected the overall manufacturability of MEMS devices. These include; *(i)* functional interfacing of the device and their standardization; *(ii)* reliability and drift issues; *(iii)* hermetic sealing techniques; *(iv)* assembly and handling techniques; and *(v)* modeling issues. A further challenge is to fabricate more devices than manipulation can facilitate. For this purpose, a parallel integration method is required that can facilitate wafer scale fabrication. This could be in-situ growth, where the nanotube is synthesized from a catalyst particle that already has been placed at the desired position in the microsystem. This has been investigated by developing and fabricating microsystems with integrated catalyst particles and by constructing and optimizing a chemical vapor deposition system for nanotube growth [16]. The fabrication techniques are essentially two dimensional while the third dimension is created by layering. MEMS components by their very nature have different and unique failure mechanisms than their macroscopic counterparts.

In comparison to electronic circuits, these failure mechanisms are neither well understood nor easy to accelerate for life testing. It is imperative that the successful design and realization of microsystems or MEMS products must include all levels of packaging and reliability issues from the onset of the project. Besides fabrication related issues, packaging encompasses several other aspects that have also affected the overall manufacturability of MEMS devices. These include; *(i)* functional interfacing of the device and their standardization; *(ii)* reliability and drift issues; *(iii)* hermetic sealing techniques; *(iv)* assembly and handling techniques; and *(v)* modeling issues.

Failure analysis of electronic packaging shows that failure usually occurs at the interconnections of dissimilar materials. With the development of IC towards high density, high speed, and small size, there is a strong demand for the high-performance microelectronic materials, especially for the physical and chemical properties of surfaces, which are the most important for high reliabilities [11].

7. FABRICATION TECHNIQUES

Microfabrication processes capable of creating three-dimensional structures in silicon were the driving force for the emergence of early MEMS devices. The evolution of these microfabrication processes has led to the classification of major micromachining techniques namely, bulk micromachining, surface micromachining, dissolved wafer process, LIGA, and electro-discharge machining [17]. The choice of the fabrication process is very im-

portant in that it defines the overall performance and cost of the micromachined part. MEMS fabrication at the manufacturing level is a very difficult task and to a large extent much more difficult than that of micro-electronics.

8. CONCLUSIONS

A good manufacturing strategy must include the complete device plan including package as part of the design and process development of the device. In spite of rapid advances in the field of MEMS there are daunting challenges that lie in the areas of MEMS packaging, and reliability testing. MEMS will open up a broad new array of cost effective solutions only if they prove to be sufficiently reliable. It is not clear if standardization of MEMS fabrication process à la CMOS will ever happen – and is even possible. But currently most of the cost for MEMS component happens during back-end process, thus it is by standardizing interfaces that most savings can be expected. MEMS fabrication is an extremely exciting endeavour due to the customized nature of process technologies and the diversity of processing capabilities. MEMS fabrication uses many of the same techniques that are used in the IC domain such as oxidation, diffusion, ion implantation, LPCVD, sputtering, etc., and combines these capabilities with highly specialized micromachining processes. One of the disadvantages of surface micromachining is that the mechanical properties of most deposited thin-films are usually unknown and must be measured. MEMS are made using IC-like processes, which enables the ability to integrate multiple functionalities onto a single microchip. MEMS borrow many of the production techniques of batch fabrication from the IC industry and therefore, the per-unit device or microchip cost of complex miniaturized MEMS can be radically reduced. IC fabrication techniques coupled with the tremendous advantages of silicon and many other thin-film materials in mechanical applications allows the reliability of miniaturized MEMS to be radically improved. Miniaturization of MEMS enables many benefits including increased portability, lower power consumption, and the ability to place radically more functionality in a smaller amount of space and without any increase in weight. The ability to make the signal paths smaller and place radically more functionality in a small amount of space allows the overall performance of MEMS to be enormously improved. In short, MEMS translate into products that have lower cost, higher functionality, improved reliability and increased performance [18]. Fabrication processes using self terminating etch stops are able to achieve better dimension control of the micromachined structures dimensions and are therefore more likely to be used in production. At manufacturing level, the degree of the difficulty of fabricating MEMS devices is highly underestimated by both the current and emerging MEMS communities.

REFERENCES

[1] M. Bâzu, et al., "Quantitative accelerating life testing of MEMS accelerometers," *Sensors*, Volume 7 (December 2007), pp. 2846-2859.

[2] T.-R. Hsu, "Reliability in MEMS Packaging," *Proc. of* the 44th International Reliability Physics Symposium, San Jose, CA, March 26-30, 2006.

[3] M. Bâzu, et al., "Modern procedures for evaluating MEMS reliability," *Quality Assurance,* Vol. XV, Nr. 57 (Jan.-March), 2009.

[4] M. Bâzu, and T. Băjenescu, *Failure Analysis – A Practical guide for Manufacturers of Electronic Components and Systems,* John Wiley, Chichester, 2011.

[5] S. A. Myhailenko, S. Luby, A. M. Fischer, F. A. Ponce, and C. Tracy, "SEM characterization of silicon nanostructures: Can we meet the challenge?" *Scanning,* Volume 30 Issue 4 (June 2008), pp. 310-316.

[6] H. Martin, and T. Daim, "Technology roadmapping through intelligence analysis: nanotechnology," *Portland Internat. Center for Management of Engineering and Technology*, 5-9 August 2007, pp. 1613-1622.

[7] D. M. Shuttleworth, *A New Failure Mechanism by Scanning Electron Microscope Induced Electrical Breakdown of Tungsten Windows in Integrated Circuit Processing*, Master of Science Thesis, University of Florida, 2002.

[8] S. J. Bae, et al., "Statistical models for hot electron degradation in nano-scaled MOSFET devices," *IEEE Trans. Reliab.,* **56**, pp. 392-400.

[9] S. K. Amakawa, Nakazato, and H. Mizuta, "A new approach to failure analysis and yield enhancement of very large integrated systems," *Proceedings of 32th European Solid-State Device Research Conference*, September 2002, Firenze, pp. 147-150.

[10] Ch. Boit, "Can failure analysis keep pace with IC technology development?", *Proceedings of 7th IPFA '99, Singapore.*

[11] T. I. Băjenescu, and M. Bâzu, *Component Reliability for Electronic Systems*, Artech House, Boston and London, 2010.

[12] Sung-Mo Kang, "Nanoscience and nanotechnology: Status, potential and roadmap," *Proceedings of 2006 Internat. Conf. on Communications, Circuits and Systems,* Vol. 2, p. 17.

[13] R. D. Gerke, *MEMS Packaging*, Chapter 8, http://parts.jpl.nasa.gov/docs/JPL%20PUB%2099-1H.pdf

[14] S. H. Voldman, *ESD Failure Mechanisms and Models*, Chapter 8, Chichester and New York: J. Wiley & Sons, 2009.

[15] F. M. Munetoshi, M. Yasuhiro, M. Yasuhiko, Y. Fumiko, and F. Takashi, "Invisible failure analysis system by nano probing system," *Hitachi Hioron,* Vol. 88 (2006)., No. 3, pp. 287-290.

[16] J. Kjelstrup-Hansen, "Integration of nanocomponents in microsystems," *4th Nanoworkshop at SDU* (University of Southern Denmark), March 8, 2007.

[17] G. L., Benavides, et al., ''High Aspect Ratio Mesoscale Parts Enabled by Wire Micro-EDM,'' *Microsystem Technologies*, 8(6), 2002, pp. 395–401.

[18] https://www.mems-exchange.org/MEMS/ fabrication.html.