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SYSTEM IDENTIFICATION APPROACH FOR EVALUATING THE THERMAL BEHAVIOUR OF PRINTED CIRCUIT BOARDS

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Abstract: *The present paper proposes a new approach for capturing the temperature gradients that occur at the Junction-To-Board level of printed circuit boards. Experiments are conducted in the first stage for evaluating the behavior of the individual heat sources. Examples include: integrated circuits, CPUs or voltage regulators. A step instruction cycle is considered to ensure the maximum amount of dissipated power. Thermal acquisition is carried out with the support of the temperature sensors that are embedded in the heat sources. The resulting temperature curves match the description of a First-Order Plus Dead Time system. Thus, the Sundaresan and Krishnaswamy method is employed for evaluating the dead time, gain and time constant of the process. The resulting transfer function can replicate the behavior of electronic packages by considering any input instruction cycle. In the next stage, a simulation model is developed comprising a simplified representation of the printed circuit board and its components. Prescribed body temperatures are considered as boundary condition for all heat sources. Subsequently, natural or forced convection cooling is included to model the interaction between the assembly and the surrounding environment. The temperature gradients can be visualized at the level of the PCB for evaluating thermal related issues. Examples include: hot spots, thermal runaway or uneven heat distribution. A practical study is included regarding the heat transfer that occurs in a Socket 462 motherboard. Opposed to existing approaches, the present methodology does not require extended knowledge in electronics heat transfer.*

Key words: *motherboard, instruction cycle, temperature acquisition, system identification, thermal analysis.*

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1. INTRODUCTION

Computer control units play an essential role in the industrial transformation of shop floor devices. Such solutions encompass a wide variety of electronic components which are attached to single or multiple Printed Circuit Board (PCB) configurations [1]. The flow of electricity through the circuits causes the release of energy under the form of heat. Based on the governing heat transfer mechanisms, a fraction of this dissipated power is transferred to the PCB [2].

Several papers address the issues of heat transfer in electronic components. One of the most common simulation procedures is the use of Computational Fluid Dynamics (CFD) software for modeling the interaction between the fluid and solid layers. In this regard, the work presented by Refai-Ahmed et al. [3] describes the use of CFD package ANSYS Icepak for the simulation of the temperature gradients occurring in a FPGA layout. A simplified representation of the heat sources is employed. Forced convection cooling takes place in an enclosed domain. Similar studies were completed by Mathew & Hotta [4] and Sedlář & Bachorec [5].

Other approaches for evaluating the heat transfer of electronic components include the use of the Finite Element Method (FEM) [6] or numeric computing environments [7]. In either case, accurate simulation results can only be achieved by having a detailed representation of the electronic packages, their relationship with the PCB and with the surrounding thermal junctions [8].

Major manufacturers provide datasheet information regarding the power dissipation of existing components. However, the values provided are derived in laboratory conditions [9] which are unlikely to occur in practice. Thus, an accurate modeling of the thermal behavior of the heat sources relies on the ability of the engineers to replicate the real world operational conditions.

The present paper proposes a new approach for the evaluation of the temperature distribution occurring in PCBs.

Experiments are conducted by applying a step input instruction cycle on the tested device. Temperatures are measured by using the internal thermocouples of the heat sources or by employing non-contact acquisition systems. The resulting variation curves are subjected to the Sundaresan and Krishnaswamy method [10] for deriving the dead time, time constant and gain of a first-

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order plus dead time system. This black box approach facilitates the simulation of the temperature increase occurring at the level of the electronic components without requiring explicit knowledge of the heat flow paths.

In the next stage, a FEM simulation model is developed comprising a layered representation of the PCB and its traces. The Junction-to-board locations are modeled by means of imprinted faces. Prescribed temperatures are applied as boundary conditions at the level of the heat sources based on the simulated signals of the First-Order Plus Dead Time (FOPDT) systems. Natural convection is defined on the horizontal plane of the PCB for capturing the exchange of heat with the surrounding environment.

The outcome of the research is to evaluate the temperature gradients for identifying thermal issues in the design stage of the PCBs by employing a simplified representation of the power dissipation and the heat transfer mechanisms.

A practical example is provided regarding the evaluation of hot spots occurring in a Socket 462 motherboard. The proposed methodology is employed for all of the active heat sources that are attached to the PCB. Only the CPU, Northbridge and Southbridge results are depicted in the paper, given their dominant power dissipation. Afterwards, the temperature distribution results from the FEM simulation are used for evaluating thermal issues at different time steps. Validation of the approach is completed by comparing experimental and simulation values that occur on the solder side of the PCB.

2. MATERIALS AND METHODS

2.1. Theoretical considerations

In electronic devices, heat generation is a consequence of electrical resistance, semiconductor junctions, switching losses and leakage currents. Multiple heat flow paths exist which are emphasized by two main junctions: the Junction-to-case and the Junction-to-ambient. From a steady state point of view, the highest operating temperature of the actual semiconductor in an electronic device is regarded as the junction temperature [11]:

$$T_j = T_a + P_d \cdot R\theta ja\,, \tag{1}$$

where: T_j is the junction temperature in degrees Celsius (°C), T_a – ambient temperature in degrees Celsius (°C), P_d – power dissipation of the component in watts (W) and $R\theta_{ja}$ is the thermal resistance from junction to ambient in degrees Celsius per watt (°C/W).

Thermal resistance represents the reciprocal of thermal conductance, or the ability of an electronic package to conduct heat. The dissipated energy must flow away from the component in order to prevent it from reaching the junction temperature.

Thermal resistance of an electronic device can be calculated as [12]:

$$R\theta = \frac{\Delta T}{P}\,. \tag{2}$$

where: $R\theta$ is the thermal resistance in degrees Celsius per watt (°C/W), ΔT – temperature difference between the junction and the ambient air in degrees Celsius (°C) and P – power dissipation of the device in watts (W).

From a transient point of view, the temperature of an electronic component occurring in an ideal operational environment can be described as [13]:

$$T(t) = T_a + P_d \cdot R\theta ja \cdot \left(1 - e^{\frac{-t}{RC}}\right), \tag{3}$$

where: $T(t)$ is the junction temperature at time t in degrees Celsius (°C), T_a – ambient temperature in degrees Celsius (°C), P – power dissipation of the component in watts (W), $R\theta_{ja}$ – thermal resistance from junction to ambient in degrees Celsius per watt (°C/W) and RC – thermal time constant of the component in seconds (s).

The thermal time constant (RC) measures how quickly the component will reach its steady-state temperature. It is calculated as the product of the thermal mass of the component and the thermal resistance of the component from junction to ambient.

While the relationships presented above are useful for developing the equivalent thermal network of a PCB, their use is limited given the fact that the behavior of the heat sources is influenced by environmental and assembly conditions such as: the layout of the electronic components, the existence of heat sinks or other cooling devices or the soldering technology employed.

Thus, a common practice in control engineering is to use black box models to approximate the thermal response of an electronic package by using FOPDT systems. Such single exponential stage models are characterized by a first-order transfer function with a dead time delay [14]:

$$G(s) = \frac{Y(s)}{u(s)} = \frac{K \cdot e^{-\theta_d \cdot s}}{\tau \cdot s + 1}\,, \tag{4}$$

where: K is the gain of the system, θ_d – dead time delay and τ – time constant of the system.

The dead time delay (θ_d) is the time it takes for the output of the system to respond to a change in the input. On the other hand, the time constant (τ) represents the time it takes for the output of the system to reach 63.2% of its final value after a step change in the input.

A system identification methodology can be employed for deriving the FOPDT constants based on experimental data. From this perspective, the approach proposed by Sundaresan and Krishnaswamy evaluates the response of the system at two times, t_1 and t_2, corresponding to 35.3% and 85.3% of the step response. The time constant of the process is calculated as [10]:

$$\tau = \frac{2}{3} \cdot (t_2 - t_1)\,. \tag{5}$$

On the other hand, the dead time is identified from:

$$\theta = 1.3 \cdot t_1 - 0.29 \cdot t_2\,. \tag{6}$$

The temperature gain can be derived from the ambient and junction temperature as:

$$K = \frac{T_j}{T_a}. \tag{7}$$

The resulting FOPDT replicates the thermal behavior of the heat source for any given instruction cycle. Thus, the temperature curves can further be used in FEM transient thermal analysis as a prescribed condition.

Conduction is the primary mode of heat transfer in electronic devices. Heat is generated in electronic components by the flow of current [15]:

$$k\left(\frac{\partial^2 T}{\partial x^2}+\frac{\partial^2 T}{\partial y^2}+\frac{\partial^2 T}{\partial z^2}\right)+q = qc\frac{\partial T}{\partial t}. \tag{8}$$

where: k represents the thermal conductivity, t – time, T – temperature, q – rate of heat flux due to internal heat generation and/or convection, ρ – density of the material.

2.2. The proposed approach

The proposed approach comprises 3 layers of abstraction: the experimental, system identification and simulation ones (Fig. 1).

In the experimental layer the studied PCB is placed in a disturbance free environment. An instruction cycle is defined to recreate a step loading condition. In this scenario, the heat sources will switch between idle to fully operational state in a short amount of time, causing their internal temperature to increase. Dedicated stress tool software can be employed for this purpose.

Temperature acquisition is carried out by using the sensors that are embedded in the electronic components. Alternatively, thermocouples can be used to capture the heat transfer occurring at the Junction-to-ambient. An infrared pyrometer can replace contact sensors when the risk of short circuit is present. The test procedure can be considered complete when the temperature of all heat sources reaches an equilibrium value.

In the system identification layer the step response of the heat sources is further used for evaluating the constants of an FOPDT system. The Sudaresan and Krishnaswamy method is employed for this purpose.

The objective of the simulation layer is to develop a FEM model that comprises a simplified representation of the PCB and its components. The temperature curves of the heat sources are extracted from the FOPDT and used as prescribed body values for the active heat sources. Natural or forced convection cooling is defined on the exterior surfaces of the PCB. The time varying temperatures and the conduction and convective heat transfer mechanisms allow evaluating the temperature distribution in any sequence of the test cycle. Thus, hot spots, thermal runaway or uneven heat distribution can be captured with ease.

2.3. The experimental setup

The experimental setup comprises a PCChips M863G motherboard that is equipped with a Socket 462 AMD Duron CPU, operating at 1600 MHz. Two 1GB DDR-266 memory modules are installed. A dedicated graphics card is included to limit the power dissipation of the CPU and Northbridge

Table 1 depicts details regarding the main heat sources that are attached to the PCB.

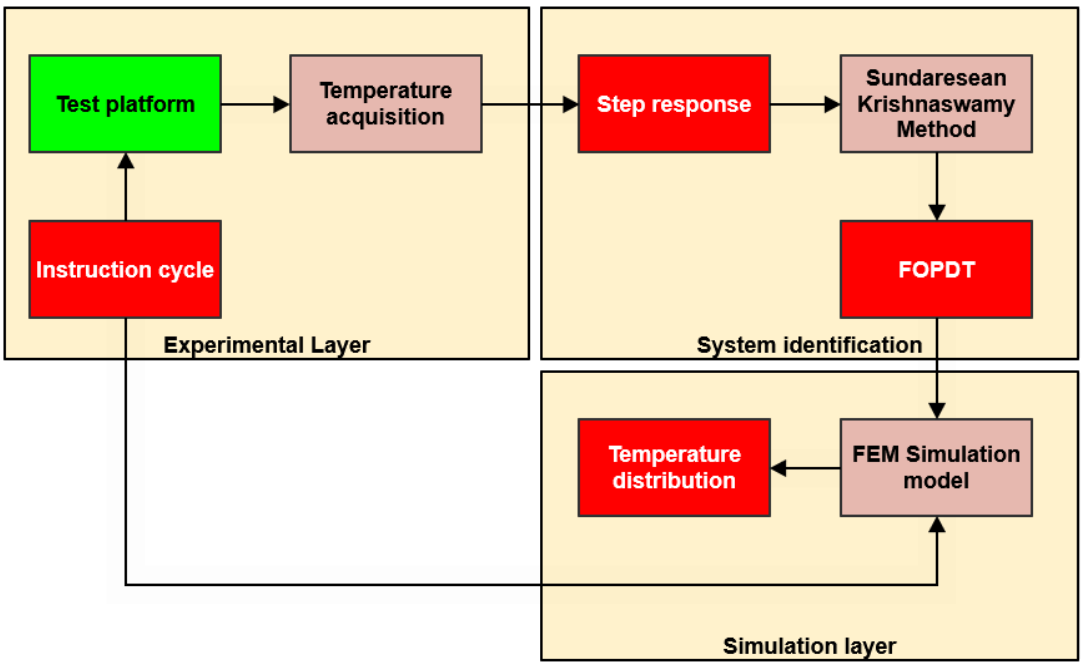

Fig. 1. Schematic representation of the proposed approach.

Table 1

Specification of the main heat sources

Name	Thermal characteristics	Specifications
CPU	Typical power dissipation 48 W / Maximum power dissipation 57W	AMD Duron Applebird 1600 MHz – 266 MHz FSB
Northbridge	5.5 °C/W Thermal resistance – Incl. heat sink	SiS 741GX – 400 MHz FSB
Southbridge	19 °C/W Thermal resistance	SiS 964L

Temperature acquisition is carried out by using the sensors embedded in the CPU. A Tc-k thermocouple is included to measure the temperatures occurring at the Sink-to-ambient junction of the remaining components. Subsequently, an infrared pyrometer captures the thermal gradients that take place at the Southbridge level.

Figure 2 depicts the layout of the experimental setup, alongside the temperature acquisition system. The instruction cycle is completed in three stages. At first, the system initializes with all components found at room temperature. Monitoring of the heat sources is carried out until the idle temperature is reached. Afterwards, a stress tool is employed to enforce the resources of the motherboard to switch to full load. Temperature acquisition takes place in this phase.

2.4. System identification

The system identification procedure is carried out in accordance with §2.1. MATLAB Simulink is employed to verify the accuracy of the FOPDT model by comparing the experimental curves with the simulated ones. The Mean Squared Error (MSE) is used as convergence metric.

2.5. The simulation layer

ANSYS Workbebch release 19.0 is employed for completing the modeling and simulation stages.

The CAD representation of the PCB and its heat sources is completed based on datasheet information in the DesignModeler interface. Each component is simplified by means of primitive representations (Fig. 3).

The material properties are defined in accordance with the specifications of the heat sources and their mounting sockets. In this regard, the thermal characteristics of the PCB are derived from [16] by considering the contribution of the PCB traces to the overall conductivity of the model (Table 2).

The density of the PCB stack-up is evaluated from its mass and volume as 5.8 g/cm^3. On the other hand, the specific heat of 1100 J/Kg°C is employed as a reference value [17].

Silicone is considered for the chips, aluminum alloy for the heat sinks, Liquid Crystal Polymer (LCP) for the expansion slots and polypropylene for the case of the chips.

Meshing is carried out by employing a hex dominant procedure. From this perspective, the bodies comprising multiple primitives were sliced and the MultiZone technique was used to generate pure hexahedral elements. On the other hand, the PCB was meshed with mixed elements, comprising both hexahedral and tetrahedral ones (Fig. 4).

Table 2

Thermal properties of the PCB

Total mass of the PCB (kg)	Mass of the PCB traces (kg)	Thermal conductivity (W/m^2°C)	
		In-Plane	Out of plane
0.301	0.0602	70.8	0.73

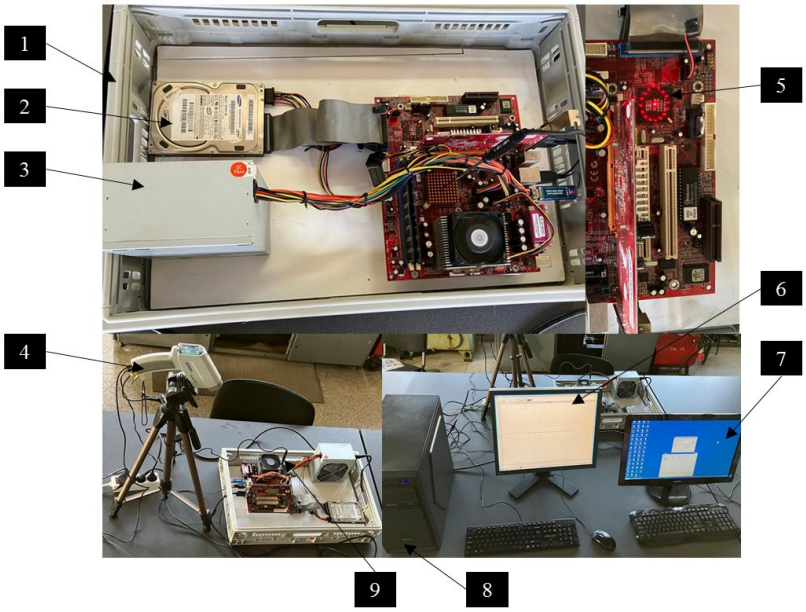

Fig. 2. Details regarding the experimental setup: 1 – Plastic tray; 2 – Hard-drive; 3 – Power supply; 4 – Raynger MX Pyrometer; 5 – Location of Southbridge temperature acquisition; 6 – LCD monitor for the acquisition PC; 7 – LCD monitor for the test platform; 8 – Acquisition PC; 9 – location of Tc-k thermocouple, on the Northbridge heat sink.

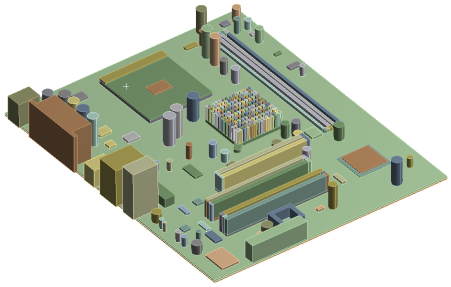

Fig. 3. Simplified CAD representation of the PCB and its heat.

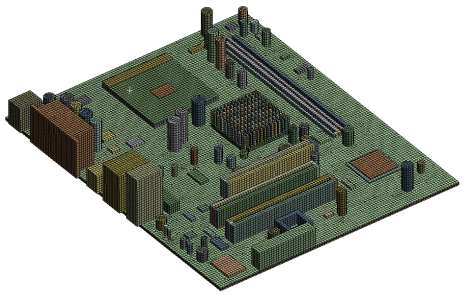

Fig. 4. The resulting mesh.

The analysis type is set to a transient thermal one. Automatic time stepping options are switched off and the substep settings are adjusted to match the acquisition rate of the experimental procedure.

The convection heat transfer is included for the horizontal surfaces of the model that are oriented upward and downward.

3. RESULTS AND DISCUSSIONS

3.1. Experimental results

Table 3 summarizes the initial and maximum temperatures of the main heat sources.

Note that the most critical values occur in case of the Southbridge, given the fact that no heat sink is included for its cooling. Thus, the power is dissipated by means of natural convection and conduction occurring at the Junction-to-case.

On the other hand, the maximum amount of heat is released by the CPU, given its forced convection cooling system. However, only a fraction of this heat reaches the PCB due to the low thermal conductivity values of the Socket 462 material.

3.2. System identification results

Figure 5 represents a comparative representation of the experimental and simulated temperature curves, derived for 311 acquisition points.

The results for the times t_1 and t_2 are depicted in Table 4.

Table 3

Temperature of the heat soruces

Heat source	Initial temperature (°C)	Maximum temperature (°C)
CPU	36	45.7
Northbridge	34	44.8
Southbridge	35.3	54

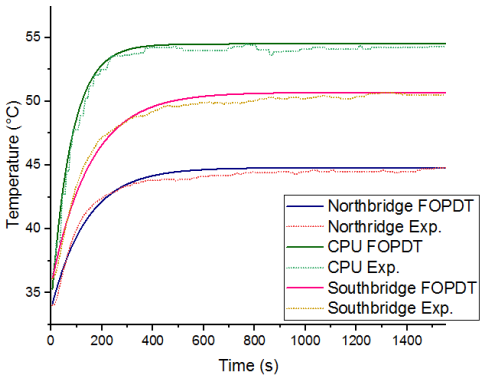

Fig. 5. Comparison between FOPDT and experimental results.

Table 4

Sundaresan and Krishnaswami results

Heat source	t_1 (s)	t_2 (s)	$T_{35.3\%}$ (s)	$T_{85.3\%}$ (s)
CPU	70	299	41.2	48.5
Northbridge	62	270	37.8	43.2
Southbridge	38	155	42	51.6

Table 5

Gain, time constant and dead time

Heat source	K	τ	θ
CPU	14.6	153.4	4.29
Northbridge	10.8	139.36	2.3
Southbridge	19.2	78.39	4.45

Table 6

Experimental and FOPDT temperature curves MSE

Heat source	MSE
CPU	0.18
Northbridge	0.14
Southbridge	0.22

Based on the results in Table 4, the temperature gain, time constant and process delay are presented in Table 5.

The MSE values are depicted in Table 6.

The results achieved prove the ability of using FOPDT for evaluating the thermal behavior of all of the heat sources that are found on the PCB, given the maximum MSE of 0.22 that was achieved for the main ones.

3.3. Simulation model results

The first step in evaluating the thermal performances of the motherboard layout consists of processing the temperature curves on the component and solder sides of the PCB. This procedure is employed in the location of the active heat sources. Figure 6 and 7 depict a comparative representation of the time vs. temperature values occurring for the CPU, Northbridge and Southbridge junctions.

In general, the thermal gradient between the two sides of the PCB is between 2.3 °C and 3 °C. However, a steep increase can be noticed in case of the Northbridge solder side. This is due to the fact that the chip transfers a large fraction of the generated heat to its case and from there to the PCB.

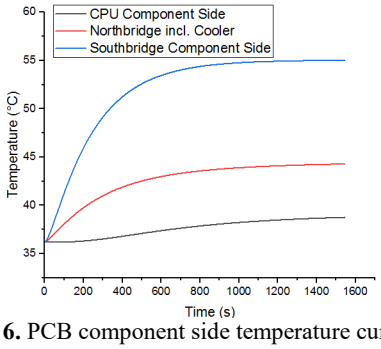

Fig. 6. PCB component side temperature curves.

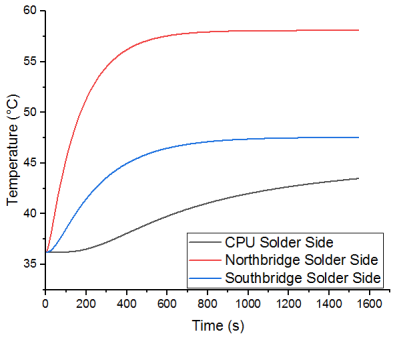

Fig. 7. PCB solder side temperature curves.

The remaining power is dissipated to the surrounding environment by means of the passive cooler. Due to the uneven thermal gradient on the component and solder sides, the lifespan of the motherboard can be reduced as a consequence of premature aging of the PCB layers.

In the next stage, the processing of the temperature distribution occurring at the PCB level at 50 and 100% of the instruction cycle is carried out. Figure 8,*a* and *b* depict the fringe plot of the component and solder sides. The areas of interest are highlighted as: the CPU, Northbridge and Southbridge. The junctions of the voltage regulators and the CJ48305 IC are also included given their temperature gradients.

It can be noticed that on the component side of the PCB the temperature distribution is even, except the location of the voltage regulators. This is due to the tightly packed layout of these components and their high power dissipation. However, a localized hot spot can be visualized at both time steps in the vicinity of the CJ48305 IC, close to the second DDR bank. This can cause performance issues and reduce the lifespan of the component. The space between the DDR memory banks and the edge of the motherboard is limited. Thus, adding additional cooling components would further reduce the available space. This is especially true given the small form factor of the studied layout.

The lack of cooling is caused by the edge distance and the existence of another heat source in the proximity of the IC.

Changes can be carried out regarding the design of the PCB for addressing the identified thermal issues. At first, the power dissipation of the Northbridge on the solder side can be adjusted by employing a higher performance heat sink that is equipped with adequate thermal interface material. Thus, more power can be dissipated at the Case-To-Heat sink junction.

The position of the voltage regulators can be adjusted to benefit more from the airflow exiting the CPU cooler. A more effective solution is to include a passive heat sink design. However, the economic aspects of the proposed layout can limit such solutions.

3.4. Validation of the given concepts

The experimental setup is extended to prove the given concepts, by attaching a thermocouple to the solder side of the PCB in the area of the CJ48305 IC. Temperature curves are extracted in the same location from the FEM simulation model.

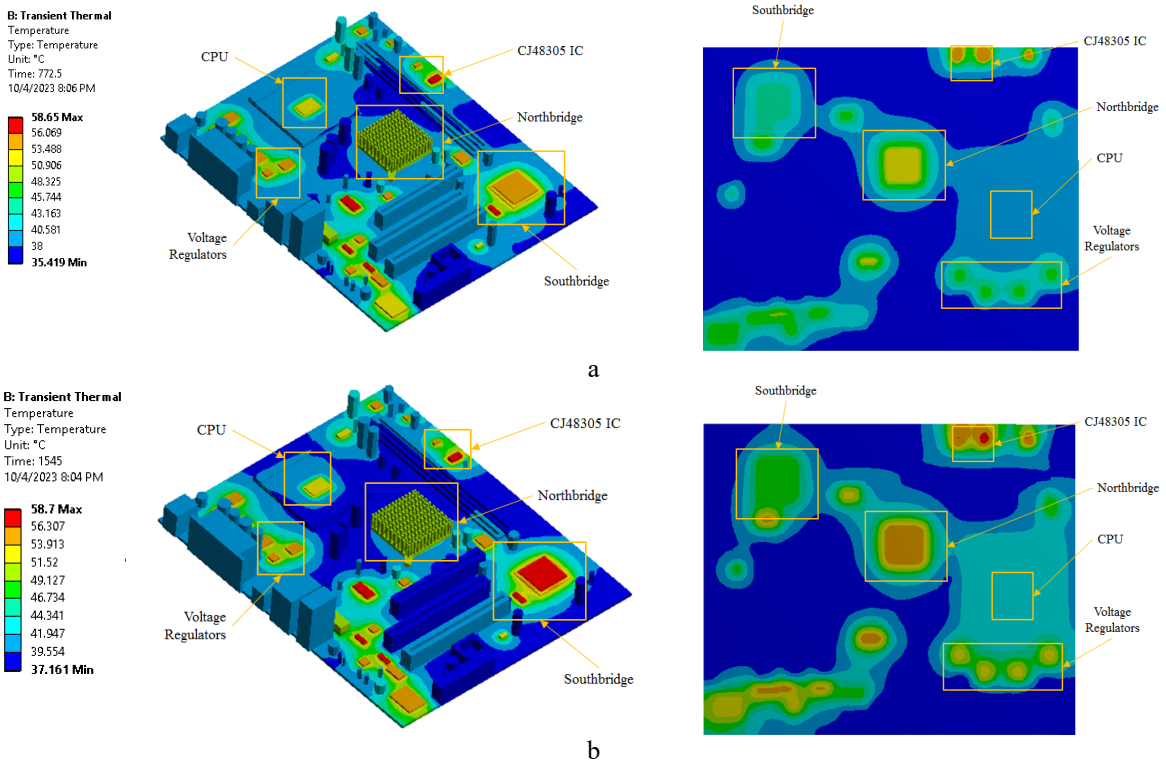

Fig. 8. Temperature distribution fringe: *a* – PCB component side, *b* – PCB solder side.

Figure 9 depicts the experimental vs. simulation values.

Table 7 represents the maximum temperature and settling time values derived from the two curves.

Table 8 represents the temperatures captured at 5 equally spaced data points for comparing the accuracy of the proposed methodology by means of percentage difference.

An average error of 3.45% can be noticed between the experimental and simulation temperature curves. The MSE was evaluated as 3.38%.

The values prove the ability of employing the methodology for capturing the temperature gradients which occur in PCB layouts. Thus, thermal issues such as hot spots or uneven heat transfer can be evaluated in the design stage of the PCB. However, the extended use of the approach for developing control methodologies or for implementing thermal management solutions is limited given the differences in the slope of the two curves. Furthermore, the FEM simulation model proves a greater dead time than compared to the experimental one.

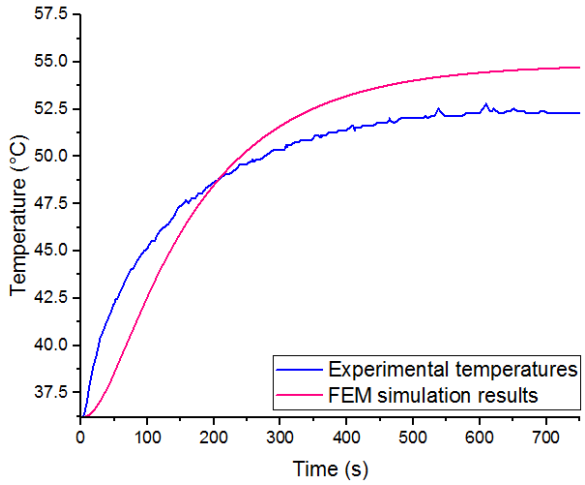

Fig. 9. Experimental vs. simulation temperature curves.

Table 7

Maximum temperatures and settling time of the two signals

Curve	Maximum temperature (°C)	Settling time (s)
Experimental	52.28	439.8
FEM	54.73	444.9

Table 8

Percentage difference between discrete data points

Time step (s)	Experimental temperature (°C)	Simulation temperature (°C)	Percentage difference (%)
151.80	47.43	46.06	2.93
303.60	50.37	51.63	2.47
455.40	51.77	53.72	3.69
607.20	52.54	54.45	3.57
759.00	52.28	54.73	4.56

4. CONCLUSIONS

The present paper proposes a new approach for capturing the temperature gradients that occur in PCBs due to the power dissipated by active heat sources.

Experiments are conducted in the first stage by considering a step input instruction cycle. The temperature of the electronic components is measured by employing their internal temperature sensors, thermocouples or non-contact acquisition methods.

Afterwards, an FOPDT system is derived from the temperature curves by employing a system identification methodology. The resulting transfer functions are used to recreate the thermal behavior of the heat sources for any given operational scenario.

A FEM simulation model is developed comprising a simplified representation of the PCB and its components. Loads are defined as prescribed temperatures from the FOPDT output while the heat transfer takes place due to conduction and convection mechanisms. A Socket 462 motherboard layout was included as case study. While no thermal issues occur in the CPU, Northridge and Southbridge proximity, a localized hot spot was visible on the FEM simulation results. The maximum temperature of 58.7 °C occurring in the location exceeds the temperatures measured at the CPU, Northbridge and Southbridge levels. Its existence was proved on the physical layout by measuring the temperatures occurring on the solder side of the PCB in the location of interest. The results achieved prove an accuracy of 3.45%, which is satisfactory for evaluating the behavior of new PCB layouts in their design stage. Moreover, the given concepts can also be applied to other PCB layouts, such as numeric control or power supply modules of industrial devices.

Changes were proposed to limit the identified thermal issues. Alternatively, a passive heat sink can be included. The hot spot that is located at both solder and component side of the PCB is a consequence of the CJ48305 IC power dissipation. The distance to edge in that location as well as the existence of another heat source in the proximity of the IC requires component repositioning for addressing the issue. However, all of these changes require a cost analysis prior to their implementation.

One limiting aspect of the proposed approach is the fact that the FOPDT model is sensitive to the thermal junctions of the electronic components. Thus, the same heat source can exhibit different temperature gain and time constant when the soldering technology or PCB layer stack up employed is different. The same can be said about thermal interface materials.

Future work will focus on lowering the error between the experimental and simulation temperature curves by developing a better understanding of the soldering and thermal interface material influence on the heat transfer.

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